Amendments to the Claims

The listing of claims will replace all prior versions, and listings of claims in the application.

1. (Previously Presented) A system comprising:

a circuit comprising an n-type transistor, the n-type transistor adapted to comply with an operational requirement;

an electrostatic discharge (ESD) protection system adapted to comply with an ESD requirement; and

a pad,

wherein the ESD protection system is connected in series between the pad and the n-type transistor, and substantially eliminates ESD from flowing from the pad into the n-type transistor, and the size of the n-type transistor and the size of the ESD protection system collectively are less than the size of a single n-type transistor adapted to comply with both the operational requirement and the ESD requirement.

2. (Canceled)

3. (Original) The system of claim 1, wherein the circuit comprises an NMOS transistor.

4. (Original) The system of claim 1, wherein the ESD protection system comprises a resistor.

5. (Original) The system of claim 1, wherein the ESD protection system comprises a n-type transistor.

6. (Original) The system of claim 1, wherein the ESD protection system comprises an NMOS transistor.

7. (Original) The system of claim 1, wherein the ESD protection system comprises a p-type transistor.

8. (Original) The system of claim 1, wherein the ESD protection system comprises an PMOS transistor.

9. (Previously Presented) A system comprising:

a pad;

a circuit comprising an n-type transistor, the n-type transistor adapted to comply with an operational requirement; and

means for protecting the circuit adapted to comply with an ESD requirement, connected in series between the pad and the n-type transistor, configured to substantially eliminate ESD from flowing to the n-type transistor from the pad;

wherein the size of the n-type transistor and the size of the means for protecting the circuit collectively are less than the size of a single n-type transistor adapted to comply with both the operational requirement and the ESD requirement.

10. (Canceled)

11. (Original) The system of claim 9, wherein the circuit comprises an NMOS transistor.

12. (Original) The system of claim 9, wherein the means for protecting comprises a resistor.

13. (Original) The system of claim 9, wherein the means for protecting comprises a n-type transistor.

14. (Original) The system of claim 9, wherein the means for protecting comprises an NMOS transistor.

15. (Original) The system of claim 9, wherein the means for protecting comprises a p-type transistor.

16. (Original) The system of claim 9, wherein the means for protecting comprises an PMOS transistor.

17. (Previously Presented) A system comprising:

a circuit comprising an n-type transistor, the n-type transistor adapted to comply with an operational requirement;

one of a NMOS transistor and a PMOS transistor system adapted to comply with an ESD requirement; and

a pad,

wherein the one of the NMOS transistor and the PMOS transistor is connected in series between the pad and the n-type transistor, and substantially eliminates ESD from flowing from the pad into the n-type transistor, and the size of the n-type transistor and the size of the one of the NMOS transistor and the PMOS transistor collectively are less than the size of a single n-type transistor adapted to comply with both the operational requirement and the ESD requirement.

18. (Previously Presented) The system of claim 1, wherein the size of the n-type transistor adapted to comply with the operational requirement and the size of the EDS protection system are collectively less than 400 μm x 8 μm.

19. (Previously Presented) The system of claim 9, wherein the size of the n-type transistor adapted to comply with the operational requirement and the size of the means for protecting the circuit are collectively less than 400 μm x 8 μm.

20. (Previously Presented) The system of claim 17, wherein the size of the n-type transistor adapted to comply with the operational requirement and the size of the one of the NMOS transistor and the PMOS transistor are collectively less than 400 μm x 8 μm.